

U.S.S.N. 10,789,527

Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical errors.

The claims have been amended to overcome Examiners rejections, recite indicated allowable subject matter, and newly drafted claims have been added.

Support for the amendments and newly drafted claims is found in the original claims and the Specification.

No new matter has been added.

For example, support for new claims 21, 22, and 24 is found in Figure 6 (item 24) and in the Specification at paragraphs 0025 and 0026.

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**BEST AVAILABLE COPY****Claim Rejections under 35 USC 112**

Claims 8-13 and 15-20 have been amended as suggested by Examiner to overcome Examiners rejection under 35 USC 112, second paragraph.

**Claim Rejections under 35 USC 102(e)**

1. Claims 1, 2, 4, 7-9, and 11, stand rejected under 35 USC Section 102(e) as being anticipated by Yan et al. (US 6,864,152).

Yan et al. discloses a method of isolating active areas of a semiconductor substrate where shallow isolation trenches are formed including overlying deep trenches. The deep trenches are formed by lining the deep trenches with an insulating liner (see item 216, e.g., Figure 3), and then filling the remaining portion with a semiconductor material (see item 218, e.g., Figure 3). Shallow trenches are then formed in a second area of the substrate as well as overlying the deep trenches (see item 224 and 224a, Figure 5, followed by filling the shallow trenches with an insulating material.

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Thus, Yan et al. does not disclose several aspects of Applicants disclosed and claimed invention including a storage capacitor.

Since Yan et al. fail to anticipate Applicants disclosed and claimed invention with respect to Applicants independent claims, neither does Yan et al. anticipate Applicants dependent claims.

2. Claims 1-4, 7-11, and 14-18 stand rejected under 35 USC Section 102(e) as being anticipated by Mehta (US 6,833,602).

Mehta discloses a device having electrically isolated high voltage regions and low voltage regions. In the device of Mehta, the high voltage isolation trench includes a wider shallow isolation portion (see item 52, e.g., Fig 4), overlying a narrower and deeper high voltage isolation portion (see item 60, Fig 4). The shallow portions of the high voltage isolation trench may be formed simultaneously with shallow low voltage isolation trenches forming a second area of the substrate (not shown; see col 6, lines 28-43). A dielectric liner is then formed to line the isolation trenches (see item 75, Fig 7). Insulating material is then deposited over the liner to fill the

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isolation trenches (see Figures 8 and 9).

Thus, Yan et al. does not disclose several aspects of Applicants disclosed and claimed invention including a storage capacitor.

Since Mehta fails to anticipate Applicants disclosed and claimed invention with respect to Applicants independent claims, neither does Mehta anticipate Applicants dependent claims.

Applicants have amended the independent claims to recite indicated allowable subject matter and overcome Examiner rejections.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

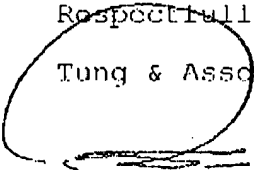
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In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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